Amendment to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1. (Presently Amended) A method of developing an ASIC ~~using a hardware model, a software, and a network, the hardware model comprising a CPU bus functional model, the software being coupled to a CPU server, and the network configured to provide communications between the hardware model and the software, the method~~ comprising ~~the steps of~~:

developing ~~the~~ a hardware model **including a CPU bus functional model** and ~~the~~ a software **coupled to a CPU server** concurrently; ~~and~~

communicating command and control information ~~directly~~ between the CPU server and the CPU bus functional model over ~~the~~ a network~~, and~~ ;

~~communicating command information directly between the CPU bus functional model and the CPU server over the network to co-simulate~~

co-simulating the hardware model and the software ~~while the hardware model and the software are being developed~~; and

receiving real working environment test inputs for the co-simulation.

Claim 2. (Previously Presented) The method of claim 1, wherein the hardware model is developed on a workstation.

Claim 3. (Original) The method of claim 1, wherein the software is developed on a target board.

Claim 4. (Presently amended) The method of claim 1, wherein the network is ~~an~~ a TCP/IP protocol **network**.

Claim 5. (Presently Amended) The method of claim 1, wherein the **co-simulated** hardware **model** ~~to be co-simulated~~ is described by a high-level language model.

Claim 6. (Canceled)

Claim 7. (Original) The method of claim 1, further comprising receiving test inputs for the co-simulation from a test tool.

Claim 8. (Presently Amended) A method of co-simulating a hardware model and a software in ASIC development, ~~the hardware model comprising a CPU bus functional model, the software being coupled to a CPU server and communicating with the hardware model via a network coupled to the CPU bus functional model and the CPU server, the method~~ comprising:

requesting an access to the hardware model **including a CPU bus functional model from a hardware component** to ~~the~~ a software **component** ~~via the~~ **coupled to a CPU server over a** network;

invoking a function call by the CPU server;

sending an access request from the **CPU** bus functional model to the CPU server ~~via~~ **over** the network;

routing the access request to the hardware model;

~~developing the hardware model and software concurrently; and~~

co-simulating the hardware model and the software ~~while the hardware model and the software are being developed.~~ **; and**

receiving real working environment test inputs for the co-simulation.

Claim 9. (Original) the method of claim 8, wherein the function call is a READ function call.

Claim 10. (Original) The method of claim 8, wherein the function call is a WRITE function call.

Claim 11. (Presently Amended) The method of claim 8, further comprising:

requesting a hardware model interrupt**[[,]];** and

~~a function call to handle~~ **handling** the **hardware model** interrupt ~~being~~ **with a function call** invoked by the software ~~via~~ **component over** the network.

Claim 12. (Presently Amended) An apparatus for hardware model and software co-simulation in ASIC development, comprising:

a hardware model~~, the hardware model representing a hardware board circuit to be co-simulated/tested, the hardware model being developed on a~~

~~workstation and~~ including a CPU bus functional model **to represent a hardware board circuit**;

a software~~, the software providing~~ **to provide** command and control access of the hardware model**;** ~~, the software being developed/debugged on a target board concurrently with a design of the hardware model, the~~

a target board including a CPU server in communication with the software; and

a network coupled ~~between~~ **to** the CPU bus functional model and the CPU server to communicate a command from the software to the hardware model and to route contents of the command between the hardware model and software~~, thereby providing~~ **to provide** co-simulation of the hardware model and software**[[.]]**

wherein the hardware model is configured to receive real working environment test inputs for the co-simulation.

Claim 13. (Canceled)

Claim 14. (Previously Presented) The apparatus of claim 13, wherein the software is loaded on the CPU server.

Claim 15. (Presently Amended) The apparatus of claim 12, wherein the network is ~~an~~ **a** TCP/IP protocol **network**.

Claim 16. (Canceled)

Claim 17. (Presently Amended) The apparatus of claim 12, wherein the hardware model is ~~**capable of receiving**~~ **configured to receive co-simulation** test inputs ~~**for co-simulation**~~ from a test tool.